IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:
Bernstein, et al.

Atty. Docket No.: BUR920010178US1

Serial No.: 10/023,235

Group Art Unit: 2128

Filed: December 17, 2001

Examiner: Saxena, Akash

For: SYSTEM AND METHOD FOR TARGET-BASED COMPACT MODELING

Commissioner for Patents
P.O. Box 1450
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REPLY BRIEF IN RESPONSE TO EXAMINER'S ANSWER

Sirs:

This REPLY BRIEF is being filed in response to the EXAMINER'S ANSWER dated June 7, 2007 and is timely filed.

I. STATUS OF CLAIMS

Claims 1-3, 5-11, 13-22, 24-38 and 40-42 are all the claims pending in the application and are under appeal. Claims 1-3, 5-11, 13-22, 24-38 and 40-42 stand rejected under 35 U.S.C. §112, first and second paragraphs. Claims 1-3, 5-11, 13-22, 24-38 and 40-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al., (U.S. Patent No. 6,269,277), hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic, further in view of applicant's own admission. Claims 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission, further in view of Peng et al. (U.S. Patent No. 6,028,994), hereinafter referred to as Peng. All rejections of all pending claims 1-3, 5-11, 13-22, 24-38 and 40-42 are appealed.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review are whether claims 1-3, 5-11, 13-22, 24-38 and 40-42 are based on a disclosure which is not enabling, whether claims 1-3, 5-11, 13-22, 24-38 and 40-42 are indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention, whether claims 1-3, 5-11, 13-22, 24-38 and 40-42 are unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission and whether claims 28-29 are unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission, further in view of Peng.

III. EXAMINER'S RESPONSES TO ARUGMENTS PRESENTED BY APPELLANTS IN APPEAL BRIEF OF JANUARY 1, 2008

A. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

(1) Examiner's Response: "Examiner thanks appellant in explaining the technology and their interpretation of the claim in remarks on Pg.55-58, however the claim 1 states:

> "A simulator comprising: a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said computer model is generated based on a target model for said device and wherein said target model is created using a *target performance parameter range* for said performance attribute and is adapted to predict process and design variations of said device; and a processor in communication with said memory and adapted to *determine said target performance parameter range* and to execute said computer model,... "

As best understood the target model is created using the target performance parameter range (see memory step), and performance parameter range are determined using the computer model (see processor step) when executed by the processor. However computer model is generated based on the target model (see memory step), thereby presenting a *cyclical problem* in building/determining which one of the computer model, target model or performance parameter range is the starting point. Therefore it would not be possible to build the target model as claimed. This problem in building the model is not addressed by appellant. Further the disclosure fails to present details of either the computer model, target model or performance parameter range *for the device/integrated*

circuit component, in the sections cited by the appellant (see specification [0023], [0025], [0026], 0035], [0036]). Hence one of ordinary skill in the art would be unable to *build and/or use the claimed invention.* For at least the reasons above examiner requests the rejection to be maintained. Claims 9, 14, 19, 24, 36, 40,4 2 present the same argument and are responded to in the same manner as above."

(2) Appellants' Reply To Examiner's Response: The Examiner's response indicates a new grounds for rejection. That is, the Examiner's Answer provides that the "disclosure fails to present details of either the computer model, target model or performance parameter range *for the device/integrated circuit component,* in the sections cited by the appellant (see specification [0023], [0025], [0026], 0035], [0036])." However, the final rejection (page 7, paragraph 16) only provided that the "the disclosure lacks enablement for creating such a computer model effectively based on performance parameters", it did not indicate that other features (i.e., the target model, etc.) were also not enabled. While it does not appear that this new grounds for rejection was approved by the Technology Center Director as required by MPEP§1207.03, the Applicant will address the new grounds herein in order to maintain the appeal. That is, the Applicants submit that the above-listed features of the present invention are properly enabled in the specification and respectfully disagree with the Examiner.

The Appellants submit that there is no such cyclical problem with the claims as presented. As discussed in the Appeal Brief, paragraph [0023] of the specification indicates that different teams are involved in the design/manufacture of a final product. A device designer creates individual devices and the circuit designer utilizes the different

devices to create a complete integrated circuit. However, problems can occur as device design progresses (see paragraph [0025]), which in turn can present a potential problem to circuit designers (see paragraph [0026]). Thus, the invention creates "a target model of the device" using target performance parameters for that device and device goals (see item 406 of Figure 4 and paragraph [0034]). More specifically, the target model is created for a device (e.g., a MOSFET) "that reflects the process performance targets that are to be achieved at the end of the process development cycle" and "is typically based on extrapolation using an existing compact model from a previous process technology" (see paragraph [0022]). Then, the "circuit design process relies upon the target performance parameters 404 for the device and the target model 406 for the device to create a circuit model 434 of the chip" [i.e., to create a computer model of the integrated circuit] (see paragraph [0035]. Next, this "circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438)" (see paragraph [0035]). Paragraph [0038] provides that this "inventive target-based compact model allows designers to evaluate variations in the process while maintaining the performance targets set out by the target model. In other words, the invention allows the designer [of a circuit] to examine how potential transistor design changes will influence representative circuits, while still maintaining the performance targets."

These features are reflected in the claims. For example, in claim 1 a memory stores "a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute". That is, the

computer model is for the integrated circuit, which comprises a device. The device comprises an integrated circuit component and further has at least one performance attribute. This computer model "is generated based on a target model for said device". The target model "is created using a target performance parameter range for said performance attribute". A processor is "adapted to determine said target performance parameter range" and also "to execute said computer model". Nowhere in the arguments presented, in the claims or in the specification do the Appellants indicate that the performance parameter range is determined using the computer model for the circuit or the target model for the device. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

B. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

(1) Examiner's Response 1: "Appellant's statement in **[1]** contradicts the following statement presented in **[2],** as no range is presented in the claim and a specific application of modeling an integrated circuit/device/component is disclosed in the claim. Further the examiner disagrees, that no specific range is required, as most of the claim is directed towards identifying the type of performance parameter (variations due to manufacturing process &device design). With so much emphasis on the performance parameter range, lack of metes and bounds makes the claim indefinite. As per **[3],** contrary to as alleged by the appellant, none of the paragraphs [0020]-[0030] or Fig.2-3 specifically teach metes and bounds of the performance parameter range. Appellant reiterates their argument on Pg.60-62 and repeats it for claims 9, 14, 19,

24,36,40,42 which are responded to in the same manner as above."

(2) Appellants' Reply To Examiner's Response 1: The Appellants previously argued "While no specific ranges are provided in the claims, none are required. The range is application specific, as claimed." Reference to the range being "application specific" meant that the first and second ranges would inevitably vary due to manufacturing process variations and the multiple model curves for different designs of the device that achieve a same performance point. Due to this variability, requiring that the Appellants claim specific ranges would unduly and unnecessarily narrow the subject matter of the invention.

Per MPEP§2173, "the primary purpose of this requirement of definiteness of claim language is to ensure that the scope of the claims is clear so the public is informed of the boundaries of what constitutes infringement of the patent." Furthermore, per MPEP §2173.02 provides that the "essential inquiry pertaining to this requirement is whether the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity." The Appellants submit that no specific range is required to be set out in the claims, as indicated by the Examiner, because the first and second bounded ranges are sufficiently defined in the claims so as to ensure that a person of ordinary skill in the art could interpret the metes and bounds of the claim so as to understand how to avoid infringement (e.g., See *Morton Int'l, Inc. v. Cardinal Chem. Co.*, 5 F.3d 1464, 1470, 28 USPQ2d 1190, 1195 (Fed. Cir. 1993). That is, given that the claims provide "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based

on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point" and "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device", a person skilled in the art would be clearly informed as to what causes infringement. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

C. REJECTIONS UNDER 35 U.S.C. § 103(A) BASED ON HERSHENSON AND KRIVOKAPIC

(1) Examiner's Response 2: "First, this limitation is in the preamble and is intended use of the target model. Secondly, Hershenson teaches performance prediction (Hershenson: Col.5 Lines 65-Co1.6 Line 13) based both on the process variation (Hershenson: Also see Col.21 Lines 19-28 - specifically addressing process variations; Col.20 Lines 6-21 where oxide thickness is process variation parameter) and design variation (Hershenson: Col.6 Lines 14-24 where topolog ies are design variation; Col.11 Lines 32-61 specifically Col.11 line 61 teaching design variation within a range of design parameters Length(Li) and Width *(Wi))* for a given model."

Appellants' Reply To Examiner's Response 2: The limitation is not in the preamble, as the preamble of claim 1 simply states "A simulator comprising". The simulator specifically comprises "a memory for storing a computer model of an

integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said computer model is generated based on a target model for said device and wherein said target model is created using a target performance parameter range for said performance attribute and is adapted to predict process and design variations of said device."

Furthermore, col. 5, line 35-col. 6, line 25, of Hershenson provides that when a new semiconductor manufacturing process is initiated on the CAD system, models for the transistors (i.e., for a single component of an IC) are generated. It does not indicate that such a target model for a device is created using a target performance parameter range for a performance attribute of the device or that the model is adapted to predict process and design variations.

Col. 20, line 6-col. 21, line 67, discusses another embodiment of the Hershenson invention for developing circuit designs. This embodiment allows circuit designs to be developed that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). The solution satisfies the specifications for all possible values of process parameters (see col. 21, lines 5-10). Reference is also made at col. 21, lines 26-54 to the fact that this embodiment can handle ranges of parameter values by specifying constraints only at endpoints. However, nowhere in col. 20, line 6-col. 21, line 67 of Hershenson does it indicate that a target performance parameter range is used to create a target model (that will subsequently be used in the generation of a circuit model), rather it only discloses that parameter values or

a range of parameter values can, in one embodiment, be plugged into a geometric programming system to provide a solution that satisfies the specifications for all possible values of the process parameters (i.e., a globally optimal circuit design).

Col. 6, lines 1-24, of Hershenson, discusses the fact that after selecting a transistor model, a circuit topology and circuit performance specifications, the system generates a geometric program for the defined performance specifications. Col. 10, line 35-col. 11, line 30 of Hershenson indicate that for a given multi-component device (e.g., an op-amp) the user determines the design parameters and performance specifications. Col. 11, line 31-col. 14, line 25 of Hershenson illustrate op-amp performance specifications and defines them in posynomial form for use in a geometric program. The cited section describes some basic constraints regarding device dimensions (e.g., the use of identical transistor pairs M1-M2 and M3-M4 in the opamp, the use of biasing transistors M5-M7-M8 with matching lengths in the opamp, lithography limitations that impose minimum and maximum sizes on the transistors, etc.). Line 61 of col. 11 specifically refers to the fact that lithography limitations and layout rules are to impose minimum and maximum sizes on the transistors. It does not indicate that a target model for a device is created using a target performance parameter range for a performance attribute of the device or that the model is adapted to predict process and design variations.

(2) Examiner's Response 3: "As per [1], appellant merely alleges that the target model is not created using a target performance parameter *range*. Examiner respectfully disagrees with appellant. Hershenson Col.5 Line 62-Co1.6 Line 24 states:

> After a transistor model has been selected, the next step in designing or optimizing a circuit is to select a circuit topology or a group of circuit topologies, step 52. A user then selects performance specifications for the desired device, such as an op-amp, step 54. The system generates a geometric program using posynomial or monomial expressions for the defined performance specifications, step 56. **[a]** The user can select one of three optimization modes. **[b]** The first mode is a standard optimization mode in which one or more performance specifications are optimized subject to a set of constraints. The second mode is a robust design mode in which in addition to the standard optimization there is an additional constraint that the design should work under several process conditions. The third mode is a trade-off curve mode. In this mode the optimization problem is repeatedly solved as the system sweeps over the range of selected constraint limits. **[c]** The output in this mode is a series of curves displaying the trade-offs of the different constraint values. For example, for an op-amp, a user can repeatedly minimize power as the system sweeps the value of the minimum required unity-gain bandwidth, and holds constant all the other constraints. The resulting curve shows the globally optimal trade-off between unitygain bandwidth and power (for the values of the other limits). The system solves the geometric program to provide the desired results, step 60. The solution provided is the globally optimal solution for the defined performance specifications. If a user selected a group of circuit topologies the system can rapidly perform the optimization analysis on each circuit topology to select the optimal circuit topology.

As seen in [a], target model is optimized with performance specifications using mathematical posynomial and monomial expressions. Further [c] teaches evaluation [performance] constraints over a range. Further, posynomial and monomial expressions are range bounded as shown in Hershenson Col.21 Lines 19-54:

> "Process variation will change the open-loop gain, making it impossible to achieve a design that yields open-loop gain of exactly 80 dB for more than a few process parameter values. The solution to this problem is to convert such specifications into inequalities. The specification might, for example, be changed to require that the open-loop gain be more than 80 dB, or that it be between 80 dB and 85 dB. **[d]** Either way the robust problem now

> has at least a chance of being feasible. It's important to contrast a robust design for a set of process parameters A=f.alpha ..sub.1,. .., .alpha ..sub.N 1with the optimal designs for each process parameter. **[g]** The objective value for the robust design is worse (or no better than) the optimal design for each parameter value. This disadvantage is offset by the advantage that the design works for all the process parameter values. So far the case in which the set A is finite has been described. But in most real cases it is infinite; for example, individual parameters lie in ranges. **[e]** As described above, such situations can be modeled or approximated by sampling the interval. While this appears to always work in practice, it gives no guarantee, in general, that the design works for all values of the parameter in the given range; it only guarantees performance for the sampled values of the parameters. in an interval. [f] ..."

As can be seen from Hershenson Col.21 Lines 19-54 [d], [e] and [f] above a clear indication is present that ranges used as input to optimize the model."

Appellants' Reply To Examiner's Response 3: The final rejection provided that both Hershenson and Krivokapic separately disclose "wherein said target model is create using performance parameter ranges for said performance attribute (HE'277: Col. 5 Lines 40-46; Also see ranges in KR'527 Fig. 1 Elements 103-107)." It further provided that Hershenson and Krivokapic both separately disclose "said target model is adapted to determine the said target performance parameter range of said device (HE'277:Col. 5 Lines 27-35; Col 6 Lines 1-48; Also See Kr'527-Fig. 1 element 109). The Appellants pointed out in the argument on page 65 of the Appeal Brief that the limitations discussed by the Examiner were not actually claimed limitations. The Appellants also pointed out that these features would necessarily be mutually exclusive and, thus, it was unclear as to how the references each separately disclosed both of these necessarily mutually exclusive features.

Reply Brief

The Examiner's Response 3 specifically refers to the following statements in the Appeal Brief: "Specifically, the claimed feature is "wherein said target model [for said device] is created using a target performance parameter range for said performance attribute [of said device]. It is not a target model that is created using performance parameter ranges for the performance attribute, nor is it a target model that is adapted to determine the target performance parameter range." The purpose of the quoted argument was to point out that the claim language referred to "a performance parameter range" and not to "target performance parameter ranges" and further to point out that the claims do not state that the target model is adapted to determine the target performance parameter range.

Additionally, the Applicants respectfully disagree with Examiner's new assertion that col. 5, line 62-col. 6, line 24 and col. 21, lines 19-54 of Hershenson disclose the target model of the present invention that is created using a target performance parameter range. Col. 5, line 62-col. 6, line 25 of Hershenson refers a system that generates a globally optimal design solution for achieving defined performance specifications. Specifically, col. 5, lines 40-46 of Hershenson indicates that "When a new semiconductor manufacturing process is initialized on the CAD system of the present invention, models for the transistors in the process are generated. The system may include posynomial transistor models of different levels of complexity that can be selected as needed based on the design requirements." Col. 5, line 61-col. 6, line 36 specifically provides that after a transistor model has been selected, the next step in designing or optimizing a circuit is to select a circuit topology or group of circuit topologies, step 52. A user then selects

performance specifications for the desired device, such as an op-amp, step 24 (i.e., for the selected circuit topology). The system of Hershenson then generates a geometric program for the defined performance specifications for the selected circuit topology, step 56. In order to perform step 56, the user selects one of three optimization modes. The solution provided is a globally optimal solution for the defined circuit performance specifications for the selected circuit topology. If the user selects a group of circuit topologies rather than a single circuit topology, the system can rapidly perform the optimization analysis on each circuit topology in the group to select the optimal circuit topology.

Col. 20, line 6-col. 21, line 67, discusses another embodiment of the Hershenson invention for developing circuit designs. This embodiment allows circuit designs to be developed that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). The solution satisfies the specifications for all possible values of process parameters (see col. 21, lines 5-10). Reference is also made at col. 21, lines 26-54 to the fact that this embodiment can handle ranges of parameter values by specifying constraints only at endpoints. However, nowhere in col. 20, line 6-col. 21, line 67 of Hershenson does it indicate that a target performance parameter range is used to create a target model (that will subsequently be used in the generation of a circuit model), rather it only discloses that parameter values or a range of parameter values can, in one embodiment, be plugged into a geometric

programming system to provide a solution that satisfies the specifications for all possible values of the process parameters (i.e., a globally optimal circuit design).

(3) Examiner's Response 4: "As per [1] appellant seems to be contradicting the claim language. Repeated again for brevity, claim 1 states:

> "A simulator comprising:
> a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said computer model is generated based on a target model for said device and wherein said target model is created using a *target performance parameter range* for said performance attribute and is adapted to predict process and design variations of said device; and a processor in communication with said memory and adapted to *determine said target performance parameter range* and to execute said computer model,... wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,"

As explained earlier, claim seem to indicate a cyclical trend where the target performance parameter range is used to create the target model, target model used to create computer model and computer model executed to determine the target performance parameter range. In plain meaning the target performance parameter range is input as well as output, where emphasis now is on the range. Arguendo, even if the appellant argument is considered, Hershenson Col.21 Lines 19-54 teaches input as range and output as series or curves displaying the tradeoff of different constraint values in Hershenson Col.6 Lines 12-14, which are ranges. This fact is elaborated on & Krivokapic (Abstract: Lines 13-16, Fig.1 and 6c showing I/V bounded curves). Please also see appellant's disclosure 2 &3 in comparison to Fig.6c right bottom.

Reply Brief

As per [2], appellant states "they [Hershenson &Krivokapic] do not go beyond that to teach the limiting feature in the present invention that the target model is created based on a *single target performance parameter range* for a given performance attribute as_claimed." Examiner respectfully disagrees, as Col.5 Line 62-Col.6 Line 24 clearly teaches optimizing multiple [performance] constraint parameters. See in Response 3 above.

Appellants' Reply To Examiner's Response 4: As mentioned above, the final rejection provided that both Hershenson and Krivokapic separately disclose "wherein said target model is create using performance parameter ranges for said performance attribute (HE'277: Col. 5 Lines 40-46; Also see ranges in KR'527 Fig. 1 Elements 103-107)." It further provided that Hershenson and Krivokapic both separately disclose "said target model is adapted to determine the said target performance parameter range of said device (HE'277:Col. 5 Lines 27-35; Col 6 Lines 1-48; Also See Kr'527-Fig. 1 element 109). The Appellants pointed out in the argument on page 65 of the Appeal Brief that the limitations discussed by the Examiner were not actually claimed limitations. The Appellants also pointed out that these features would necessarily be mutually exclusive and, thus, it was unclear as to how the references each separately disclosed both of these necessarily mutually exclusive features.

The Examiner's Response 4 directly refers to the following statements in the Appeal Brief: "Furthermore, the target model features cited in the Office Action as being disclosed by the prior art references are, by definition mutually exclusive. That is, the model can either be created using the range or it can determine the range, but not both

(i.e., you can not determine the range with the model, if you actually need it in order to create the model)." The purpose of these statements was to point out to the Examiner that using the target model to determine the target performance parameter range model is NOT a claim limitation, nor could it be because the target model is created using the target performance parameter range. That is, a circuit model that was created using a target model for a device necessarily could not be used to determine target performance parameter range for a performance attribute of a device. Consequently, it is unclear as to why the final rejection indicated that both Hershenson and Krivokapic separately disclosed "wherein said target model is created using performance parameter ranges for said performance attribute " and "said target model is adapted to determine the said target performance parameter range of said device" (even if these weren't claimed limitations) or how such would be possible.

(4) Examiner's Response 5: "Appellant is arguing a target model for a device (which is a component of an integrated circuit), contrary to claimed limitation where the device comprises an integrated circuit component (see claim 1 preamble). In either case, Hershenson teaches a device as an operational amplifier (in short opamp - Hershenson Col.5 Lines 62-67) and optimization of component performance constraints like length and width of transistor model (component) in the op-amp device (Hershenson: Col.11 Dimension Constraint section where the length and width of transistors are optimized as presented in range. see Eq.7 specifically).

Appellants' Reply To Examiner's Response 5: The claim language refers to "an integrated circuit comprising a device that comprises an integrated circuit component" (i.e., the device is a component of the integrated circuit). Thus, the Appellants' submit that the statement in the Appeal Brief to the effect that the device is a component of an integrated circuit is not contradictory.

Additionally, as discussed above, col. 5, line 61-col. 6, line 36 of Hershenson teaches that, after selecting a transistor model (i.e., a device model), a circuit topology is selected, desired performance specifications for the selected circuit topology are identified, a geometric program for the desired performance specifications is generated according to a selected optimization mode to provide a globally optimal solution for the defined performance specifications. Col. 11, line 31-col. 14, line 25 of Hershenson refers specifically to op-amp performance specifications and defines them in posynomial form for use in a geometric program. The cited section describes some basic constraints regarding device dimensions for the op-amp circuitry (e.g., the use of identical transistor pairs M1-M2 and M3-M4 in the opamp, the use of biasing transistors M5-M7-M8 with matching lengths in the opamp, lithography limitations that impose minimum and maximum sizes on the transistors, etc.). Line 61 of col. 11 specifically refers to the fact that lithography limitations and layout rules are to impose minimum and maximum sizes on the transistors. It does not indicate that a target model for a device (i.e., a circuit component) is created using a target performance parameter range for a performance attribute of the transistor or that the model is adapted to predict process and design variations.

(5) Examiner's Response 6: "This teaching is mapped/presented in Hershenson. Secondly, Page 28 Krivokapic also teaches using various values from the range to create and simulate the target model (See Krivokapic: Fig.1 &3). Further, the rejection is made under 35 USC 103, using obviousness argument and appellant is performing piecemeal analysis.

Appellants' Reply To Examiner's Response 6: As mentioned above, the final rejection provided that both Hershenson and Krivokapic separately disclosed "said target model is create using performance parameter ranges for said performance attribute" and "said target model is adapted to determine the said target performance parameter range of said device". The Appellants pointed out on page 65 of the Appeal Brief that neither of these features was actually claimed and also that neither reference taught the claimed limitation of "wherein said target model [for said device] is created using a target performance parameter range for said performance attribute [of said device]".

Specifically, the Appellants discussed Hershenson in the first paragraph of page 66 and Krivokapic in the second paragraph of page 66. In the Examiner's Response 6, page 28 of Krivokapic is referenced. However, the published patent only has 22 pages, including the drawings. Thus, it is unclear as to what portion of Krivokapic is being referred to. Furthermore, the Appellants respectfully disagree with the assertion that Krivokapic "teaches using various values from the range to create and simulate the target model (See Krivokapic: Fig.1 &3)." As mentioned above, Figure 1 refers to a prior art

method for modeling the IV curves of a device using the five-corners measured parameters (or parameters derived from measured parameters) from the same type device manufactured under various different process conditions (see col. 3, lines 5-40). It does not create a target model for a device (which is a component of an integrated circuit) using a target performance parameter range for a given performance attribute of that device. Figure 3 builds on the idea of Figure 1 and illustrates an apparatus that designs circuits in view of discovered worst case I/V curves (i.e., the simulated results) of simulated mass-produced semiconductors.

(6) Examiner's Response 7: "First bounded ranges are taught by Hershenson Col.21 Lines 19-54. See Response 3 for detailed response and highlighted teachings of Hershenson. The first bound range represents, range of performance parameter variations due to manufacturing process which is taught by Hershenson Col.21 Lines 19-54. See Response 3 underlined section **[g]** from teaching of Hershenson Col.21 Lines 19-54."

Appellants' Reply To Examiner's Response 7: The final rejection asserted that col. 7, line 1-59; col. 20, lines 6-21; col. 21, lines 10-3; and col. 20, lines 35-41, of Hershenson, teach the multiple first bounded ranges feature of the present invention. The Appellants respectfully disagreed. Specifically, the Appellants indicated on page 67 of the Appeal Brief that Hershenson at col. 7, lines 1-5, indicates the invention optimizes circuit design by modeling circuit operation using geometric programs and solving the geometric programs to provide optimal design parameter

values. Col. 7, lines 5-59, describes generally that a geometric program is an optimization problem having a specified form without references to what variables are used in the equations or what they solved for. Col. 20, line 6-col. 21, line 67, discusses an additional embodiment of the invention where the method is for developing a circuit design that meets a set of specifications for a set of values of parameters rather than specifications for known or fixed parameters. In conclusion the Appellants indicated that *the set* of specifications for *the set* of values of parameters that is taught by Hershonson does not amount to the *multiple bounded first bounded ranges* (each of which comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point) included in the target performance parameter range of the claimed invention.

In response to this argument, the Examiner has apparently conceded that the previously cited portions of Hershenson (i.e., col. 7, line 1-59; col. 20, lines 6-21; col. 21, lines 10-3; and col. 20, lines 35-41) do not teach the claimed feature of multiple first bounded ranges. Thus, the Examiner's Response 7 indicates that "First bounded ranges are taught by Hershenson Col.21 Lines 19-54. See Response 3 for detailed response and highlighted teachings of Hershenson. The first bound range represents, range of performance parameter variations due to manufacturing process which is taught by Hershenson Col.21 Lines 19-54. See Response 3 underlined section **[g]** from teaching of Hershenson Col.21 Lines 19-54."

Reply Brief

As discussed above, col. 20, line 6-col. 21, line 67, discusses another embodiment of the Hershenson invention for developing circuit designs. This embodiment allows circuit designs to be developed that meet a set of specifications for a set of values of process parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). The solution satisfies the specifications for all possible values of process parameters (see col. 21, lines 5-10). Reference is also made at col. 21, lines 26-54 to the fact that this embodiment can handle ranges of parameter values by specifying constraints for the geometric program only at endpoints. Thus, the cited portion of Hershenson only discloses that parameter values or a range of parameter values can, in one embodiment, be plugged into a geometric programming system to provide a solution that satisfies the specifications for all possible values of the process parameters (i.e., a globally optimal circuit design). It does not teach or disclose a target performance parameter range as in the present invention that comprises multiple first bounded ranges (each first bounded range comprising a range of performance parameter variations due to manufacturing process variations and being based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point) and a second bounded range (the second bounded range being constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device).

(7) Examiner's Response 8: "Appellant is alleging values of parameters, e.g. transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages correspond to specification for a circuit and not specification for a device like transistor. Appellant is incorrect, e.g. transistor threshold voltages is the voltage when transistor would turn on. Similarly [electron] mobilities, [gate oxide] oxide parameters, [CMOS] channel modulations parameters are parameters associated with MOS transistor. Circuit parameters are for the circuit built by transistor components e.g. an operational amplifier (op-amp) having parameters like open loop gain 3dB bandwidth (Hershenson: Col. 10 Lines 48-Co1.11 Line 30)."

Appellants' Reply To Examiner's Response 8: As indicated by the Examiner, the statement in the Appeal Brief on page 68 to the effect that "the referred to values of parameters (e.g., transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages, and load capacitances) correspond to specifications for a circuit and not to the specifications for a device (e.g., a transistor)" was made in error. However, as discussed in detail above, the Appellants still maintain that the parameters or range thereof referred to in the cited portions of Hershenson do not disclose the target performance parameter range of the present invention that comprises multiple first bounded ranges (each first bounded range comprising a range of performance parameter variations due to manufacturing process variations and being based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point) and a second bounded range (the second bounded range being constrained by at least two of said multiple model curves so as to

comprise performance parameter variations between said multiple different designs for said device).

(8) Examiner's Response 9: Examiner respectfully disagrees, Hershenson teaches that the target model for a device (e.g. transistor - Hershenson Col.11 Lines 40 - Co1.12 Lines 55) within an integrated circuit (e.g. operational amplifier Fig.3 having MOS transistors) is created using a target performance parameter range for a performance attribute of the device (Co1.5 Lines 61-Co16 Lines 36). Response 3 &4 disclose in detail mapping for first bounded range.

Appellants' Reply To Examiner's Response 9: Examiner's response 9 refers directly to the statement on page 68 of the Appeal Brief to the effect that "Hershenson does not teach or suggest that the target model for a device within an integrated circuit is created using a target performance parameter range for a performance attribute of the device, much less that this target performance parameter range of the device's performance attribute comprises "multiple first bounded ranges"". Please see Appellants' Reply To Examiner's Response 7, which addresses this issue.

(9) Examiner's Response 10: "Appellant alleges that target model of device (transistor) is not created using target performance parameter range, and Hershenson teaches only after selecting the transistor model to select from topologies (various designs) and performance specification (Hershenson: Col.5 Lines 61-Co16 Lines 36). Appellant is merely arguing the limitation without providing how this is different

than what is claimed. There is no disclosure present that teaches specifically how a target model of device is created using target performance parameter range. As for second bound range represents performance parameter variations between multiple different designs for the device which is taught by Hershenson (Co1.5 Lines 61-Co16 Lines 36) as topologies and also maps the output of simulation based on these topologies."

Appellants' Reply To Examiner's Response 10: Examiner's response 10 refers directly to the statement on page 68 of the Appeal Brief to the effect that "Thus, Hershenson does not teach or suggest that the target model for a device (i.e., for a component of the integrated circuit) is created using a target performance parameter range for a performance attribute of the device, much less that the target performance parameter range of the device's performance attribute comprises both "multiple first bounded ranges" and "a second bound range"". Prior to this statement the Appellants explained, that in Hershenson a single transistor model is simply selected from a library for inclusion in a circuit and then circuit topology is also selected (see col. 5, lines 63-65). That is, Hershenson only teaches selection of a transistor model, selection of a circuit topology, and describing the specifications for the selections as posynomial functions to generate a geometric program that can be solved to determine an optimal solution. Hershenson does not disclose that multiple different designs for the transistor are used in the creation of a "target model", prior to circuit modeling. More specifically, Hershenson does not teach the creation of a target model for a device, using a target performance parameter range that comprises multiple first bounded ranges (each first bounded range comprising a range of performance parameter variations due to

manufacturing process variations and being based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point) and a second bounded range (the second bounded range being constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device). Nor does it teach that such a target model is then used to generate a circuit model for an integrated circuit that comprises the device.

(10) Examiner's Response 11: "As per [1], please see Hershenson Col.20 Lines 5-Co1.21 line 51 at least. Both the design and (manufacturing) process parameters are varied (Co1.20 Lines 22-34) to achieve a performance point (Co1.21 Lined 19-27) within a specified range. As per [2], design parameters are also varied (as shown in response to [1] above and Col.11 Lines 40-66) to achieve a common goal for a performance point. e.g. 80- 85 dB open loop gain on an operation amplifier (Co1.21 Lined 19-27).

Appellants' Reply To Examiner's Response 11: In the final rejection, the Examiner indicated that Hershenson teaches "each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point (HE'277:Col. 20 Lines 6-21, Col. 21 Lines 10-60; Also See Col. 20 Lines 27-60; performance point Col. 21 Lines 35-49)." The Appellants respectfully disagreed.

In response the Appellants explained that Hershenson at col. 20, line 6-col. 21, line 67, discusses a method of developing circuit designs that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). Thus, the Appellants concluded that nothing in the cited portion of Hershenson indicates that each one of multiple first bounded ranges comprises "a range of performance parameter variations due to manufacturing process variations", much less that each one is "based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point."

The Examiner's response 11 refers specifically to this conclusion, but do not reflect the claimed limitations. Specifically, what is claimed is "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range" and "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point". Hershenson may consider varied design and process parameters to achieve a performance point within a specified range or that design parameters are varied to achieve a common goal for a performance point, but the performance point referred to is that of the resultant circuit (i.e., a circuit design that is specified to have an open-loop gain of exactly 80dB, over 80dB, etc.) and not of a component device thereof. Furthermore, the idea that ranges are bound based on multiple modeling curves corresponding to multiple designs for a device is not disclosed.

(11) Examiner's Response 12: "Hershenson states using multiple topologies which are multiple designs as in Col.6 Lines 20-24: The solution provided is the globally optimal solution for the defined performance specifications. If a user selected a group of circuit topologies [designs] the system can rapidly perform the optimization analysis on each circuit."

Appellants' Reply To Examiner's Response 12: In the final rejection, the Examiner indicated that Hershenson teaches "each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE '277: Col. 6 Lines 1-24). The second bounded range is constrained by these curves. The Applicants respectfully disagreed.

Col. 6, lines 1-24, of Hershenson, discusses the fact that after selecting a single transistor model, a circuit topology and circuit performance specifications, the system generates a geometric program for the defined performance specifications and solves the program to provide a globally optimal circuit design. If a user selected a group of circuit topologies the system can rapidly perform the optimization analysis on each circuit topology. Thus, the cited portion of Hershenson discloses selection of different circuit topologies (or different circuit designs), after the selection of a single transistor model for inclusion in the circuit topologies. However, it does not disclose creation of a target model based on multiple different device designs directed to a variation of a single design for the circuit and then generating a circuit model based on this target model.

(12) Examiner's Response 13: "As per [1], The second bounded range is device parameters (col. 6, lines 1-24) based on topologies, and further design features as length and width of the transistors (Co1.11 Lines 32-66). The length and width, min and max values disclosed on the Col.11 Eq.7 determine the current in the various equations 9, 10 and 11. These current biases having lower and upper bounds can be used in geometric programming (model) (Co1.12 Lines 57-63). These lower and upper ranges represent a bounded range for voltages (Co1.12 Line 64- Col.15 Line 25). As per [2], for multiple model curves, these are evident from Krivokapic (Abstract, Fig.1, Fig.3 element 307, Fig.6c) showing current-voltage curves, based on device simulator (Fig.6c Element 640) and design parameters (Fig.3 element 306). No new arguments are presented for dependent claims 2-3 and 5-8.

Appellants' Reply To Examiner's Response 13: The claimed feature is "wherein said second bounded range [of the target performance parameter range that is used to create the target model for the device] is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device". It is still unclear as to how this second bounded range is disclosed in the prior art references. In the final rejection, at page 10, lines 2-4, the Examiner cited col. 5, lines 40-48 as disclosing the second bounded range. Later in the final rejection at page 10, lines 14-17, the Examiner cited col. 11, lines 40-col. 12, line 61 as disclosing the second bounded range. Now it appears that various different portions of Hershenson (e.g., col. 6, lines 1-24; co1.11, lines 32-66; col.11, eq.7; col. 12, lines 57-63; and co1.12, line 64- col.15, line 25), each of which mentions some sort of a range with

upper and/or lower bounds. For example, col. 11, lines 32-66 and eq. 7 refer to lithography limitations and layout rules that impose minimum and maximum sizes on transistors. Similarly, col. 12, lines 57-63 refers to bias currents for transistors which can be expressed in monomial form in the geometric program with lower or upper bounds included. However, in Hershenson these ranges are simply expressed as constraint functions in a geometric program. They are not used in defining a target performance parameter range to create a target model for a device, which in turn is used to generate a circuit model.

Furthermore, none of these cited portions of Hershenson discloses a bounded range that is constrained by at least two of multiple model curves for different designs of a device so as to comprise performance parameter variations between the multiple different designs the device. Thus, in Response 13, the Examiner cites the worst-case I/V curves generated by the simulator in Krivokapic.

The Appellants submit that the multiple simulated worst-case I/V curves of Krivokapic are determined based on the 5 sets of parameters 103-107 associated with a particular CMOS device being manufactured under different process conditions and not with different designs of a device. That is, Krivokapic does not disclose multiple model curves for different device designs. It only discloses that after performing a simulation to generate such I/V curves, design attributes may be analyzed and varied in order to meet manufacturing tolerance guards or design specification (see col. 6, lines 42-47).

Furthermore, there would be no motive to combine the geometric programming method of Hershenson with the simulated worst-case I/V curves associated of

Krivokapic. Specifically, to determine a globally optimal circuit design, Hershenson expresses the objective and constraint functions as functions of x (design parameters) and a (process parameters, such as the parameters 103-107 of Krivokapic) (see discussed in col. 20, lines 20-26 of Hershenson). Since the geometric programming method of Hershenson works directly with the process parameters, there would be no reason for Hershenson to consider the simulated worst-case I/V curves of Krivokapic.

(13) Examiner's Response 14: "The system in claim 1 includes memory and processor to execute model stored in the memory. This limitation is mapped to Hershenson Col.6 Lines 49-52. This limitation also teaches designing a product to perform the function of the claim 1. Remaining arguments presented for claim 9 are responded to in the same manner as claim 1. No new arguments are presented for dependent claims 10-11 and 13."

Appellants' Reply To Examiner's Response 14: The Examiner's Response 14 relates to independent claim 9 and the Appellants' argument presented on pages 71-72 of the Appeal Brief. The Appellants argued that claim 9 included the additional designing feature not included in claim 1 and not taught by the cited prior art references. Specifically, claim 9 references "a product having a device comprising an integrated circuit component" and "designing said product using a computer model that is based on a target model of said device." The Response 14 indicates that such a designing feature is disclosed at col. 6, lines 49-52 of Hershenson. The cited portion of Hershenson refers to an exemplary computer system on which the CAD invention of Hershenson can be

implemented. Hershenson clearly discloses a design process. However, the Appellants submit that it does not disclose designing a product based on a computer model that is in turn based on a target model of a device and, more specifically, where the target model has the unique features claimed.

(14) Examiner's Response 15: "As per [1], Hershenson is used to show device model based on the performance parameters (constraints bounded by ranges in Col.11 Line 31-Co1.14 Line 25, specifically eq.7). Further the model is used to construct a product (Hershenson: e.g. operational amplifier Col.6 Lines 13-24; Krivokapic Fig.6a Co1.9- 11 - showing modeling of semiconductor process and device like operational amplifier - specifically Col. 10 Lines 53-58). As per [2], the product goal is optimization performed for the operational amplifier (Hershenson: Col. 10 Lines 48-Co1.11 Line 30), and device goal optimization is performed on the transistor (Hershenson: Col.11 Lines 40-Line 66; Col.20 Lines 7-67 at least). As per [3], appellant merely alleges the distinction, and fails to specifically point to which claim the argument applies. No new arguments are presented for dependent claims 15-18. Remaining arguments presented for claim 14 are responded to in the same manner as claim 1.

Appellants' Reply To Examiner's Response 15: The Examiner's Response 15 relates to independent claim 14 and the Appellants' argument presented on pages 72-73 of the Appeal Brief. The Appellants argued that claim 14 included the additional designing feature not included in claim 1 and not taught by the cited prior art references, namely: (1)"developing device goals for said device, wherein said device goals are based

on product goals;" (2) "producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device;" and (3) "designing said product with said device based on said target model."

In the final rejection, the Examiner asserted that Krivokapic "teaches developing a device and product based on the target model (KR'527:Fig.6A, Col.9-11 Section III). The goals for the product are interpreted as the same goal, as indicated in the preamble "a product comprising a device" show that the product only has one device. Although "comprising" does not limited the scope, design goals can be seen in HE'277 (Col. 6 Lines 1-24)." The Appellants respectfully disagreed and presented the argument cited by the Examiner in the Examiner's Response 15.

The Examiner appears to concede that Krivokapic does not teach developing a device and product based on a target model and, thus, cites Hershenson col. 11, lines 31-col. 14, line 25, specifically eq. 7). The Appellants respectfully disagree with the assertion that Hershenson teaches the claimed target model (see Appellants' Reply To Examiner's Responses above regarding the claimed target model). The Appellants concede that the transistor design parameters and op-amp performance specifications of Hershenson may be interpreted as device goals and product goals, respectively. It should also be noted however that the Appellants do not agree with the assertion by the Examiner that both Krivokapic and Hershenson design a product with a device based on a target model of the device, where the target model is not simply a transistor model but

rather has the unique features of the target model, as claimed (see Appellants' Reply To Examiner's Responses above regarding the claimed target model).

It should be noted that the Examiner's remark [3] cited quote from pages 72-73 is found under the heading "(3) Independent Claim 14) and, thus, clearly relates to independent claim 14. Particularly, Appellants pointed out that the preamble of independent claim 14 refers to "a method of developing a product comprising a device with at least one performance attribute" and the fact the claim limitations (e.g., "developing device goals for said device, wherein said device goals are based on product goals" and "designing said product with said device based on said target model") clearly indicate that the product and device are separate and distinct from each other and that ultimately the product is designed to include the device.

(15) Examiner's Response 16: "The product goal is optimization performed for the operational amplifier (Col. 10 Lines 48-Co1.11 Line 30), and device goal optimization is performed on the transistor (Co1.11 Lines 40-Line 66; Col.20 Lines 7-67 at least). Appellant merely alleges that the limitations in claim 24 are not taught. Remaining arguments presented for claim 24 are responded to in the same manner as claim 1. No new arguments are presented for dependent claims 25-25.

Appellants' Reply To Examiner's Response 16: See Appellants' Reply To Examiner's Response 15.

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(16) Examiner's Response 17: "As per [1], examiner disagrees with appellant, as set of subroutines is a program product to be statutory, which is taught by Hershenson Col.22 Lines 1- 21. As per [2], Please see Response 2 above and also Hershenson Col.20 Lines 22-27 stating: ...".

Appellants' Reply To Examiner's Response 17: Hershenson discloses the use of subroutines, where objective and constrain functions are expressed as functions of design and process parameters. However, the Hershenson set of subroutines is not created using the claimed target performance parameter range. See Appellants' Reply To Examiner's Response 7.

(17) Examiner's Response 18: "As per [1], examiner is rejecting one embodiment of the "performance parameter" as defined by the specification [0018]. As per [2], examiner does not see how the product could be chemical components and subcomponents of drugs, or the insole of a shoe, or the foam insulator of a hot tub, when the claim is specifically directed towards model of an integrated circuit and system,

Appellants' Reply To Examiner's Response 18: On page 78 of the Appeal Brief, the Appellants objected to the claim interpretation set out by the Examiner in paragraphs 8-11 of the final rejection. The Examiner's Response 18 specifically refers to the paragraph on pages 78-79 of the Appeal Brief related to the Examiner's interpretation of the phrase "performance parameter".

The first sentence of the paragraph indicates that the "Appellants submit that performance parameter and performance attribute, as defined in the specification, are not limited to a "current voltage switch-point" of a transistor computer model." The second

sentence supports this statement citing paragraphs [0017]-[0018]. In response, the Examiner states "examiner is rejecting one embodiment of the "performance parameter" as defined by the specification [0018]." It is unclear as what the Examiner means by "rejecting one embodiment of the performance parameter".

The remaining portion of this paragraph provides as follows:

> Examples, include chemical components and subcomponents of drugs, or the insole of a shoe, or the foam insulator of a hot tub. In each example, the former is the "device" and the latter is the "product"." The "manufacturing process can be developed to optimize certain "performance parameters" of the device. In our examples a "performance parameter" could be the current-voltage switchpoint of a transistor; solubility of a component of a drug; the rigidity of an insole; or the coefficient of thermal expansion of foam insulator for a hot tub." Thus, the term performance parameter is not limited specifically to the current voltage switchpoint of a transistor, it could be any other parameter of any other device that could be used to "help determine the functionality of the integrated product."

The Examiner has remarked "examiner does not see how the product could be chemical components and subcomponents of drugs, or the insole of a show, or the foam insulator of a hot tub, when the claim is specifically direct towards model of an integrated circuit and system, method and program product thereof." The claims, as presented, refer to a device comprising an integrated circuit component. However, the purpose of mentioning the other examples in the argument was to reiterate that the disclosure did not limit the invention to a transistor and a circuit that includes the transistor, nor did the disclosure further limit the performance parameter to a voltage switchpoint of a transistor.

(18) Examiner's Response 19: "Specification [0020]-[0030] does not include any indication of the second bound range clearly specifying it metes and bounds. The suggested curves are placeholder values which do not specify the metes and bounds. Appellant is requested to provide a clear range."

Appellants' Reply To Examiner's Response 19: As mentioned above, on page 78 of the Appeal Brief, the Appellants objected to the claim interpretation set out by the Examiner in paragraphs 8-11 of the final rejection. The Examiner's Response 19 specifically refers to the paragraph on page 79 of the Appeal Brief related to the Examiner's interpretation of the phrase "second bounded range". Specifically, the Appellants indicated that paragraph [0020] of the specification indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range that is constrained by at least two variables (i.e., within a target performance parameter range that is constrained by two variables). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] of the specification explains that variations in a design of a device, which still achieve the same performance point, may results in different model curves. These model curves are illustrated as curves 20-22 in Figure and represent multiple different designs for the same device. As explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20. This reflects the second bounded range, as claimed. See also Appellants' Reply To Examiner's Response 1.

IV. CONCLUSION

In view the forgoing, the Board is respectfully requested to reconsider and withdraw the rejections of claims 1-3, 5-11, 13-22, 24-38 and 40-42. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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